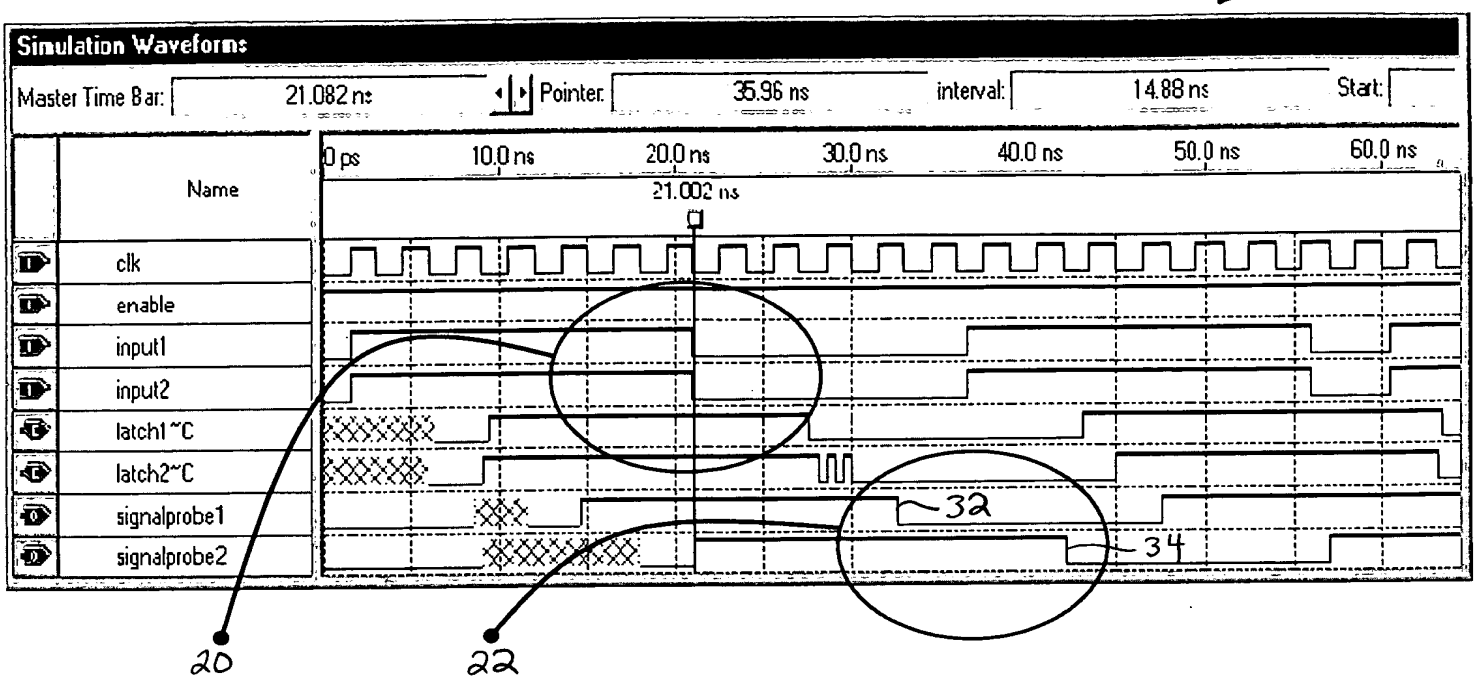
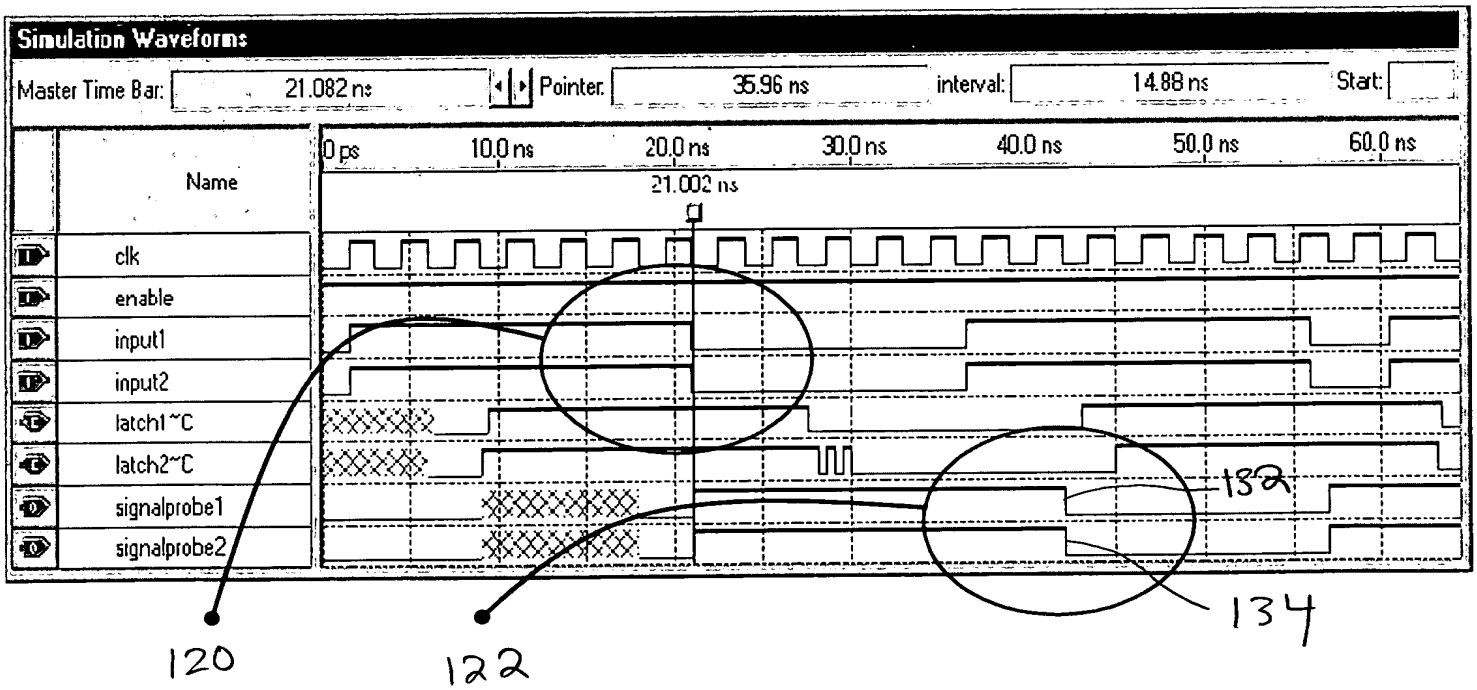
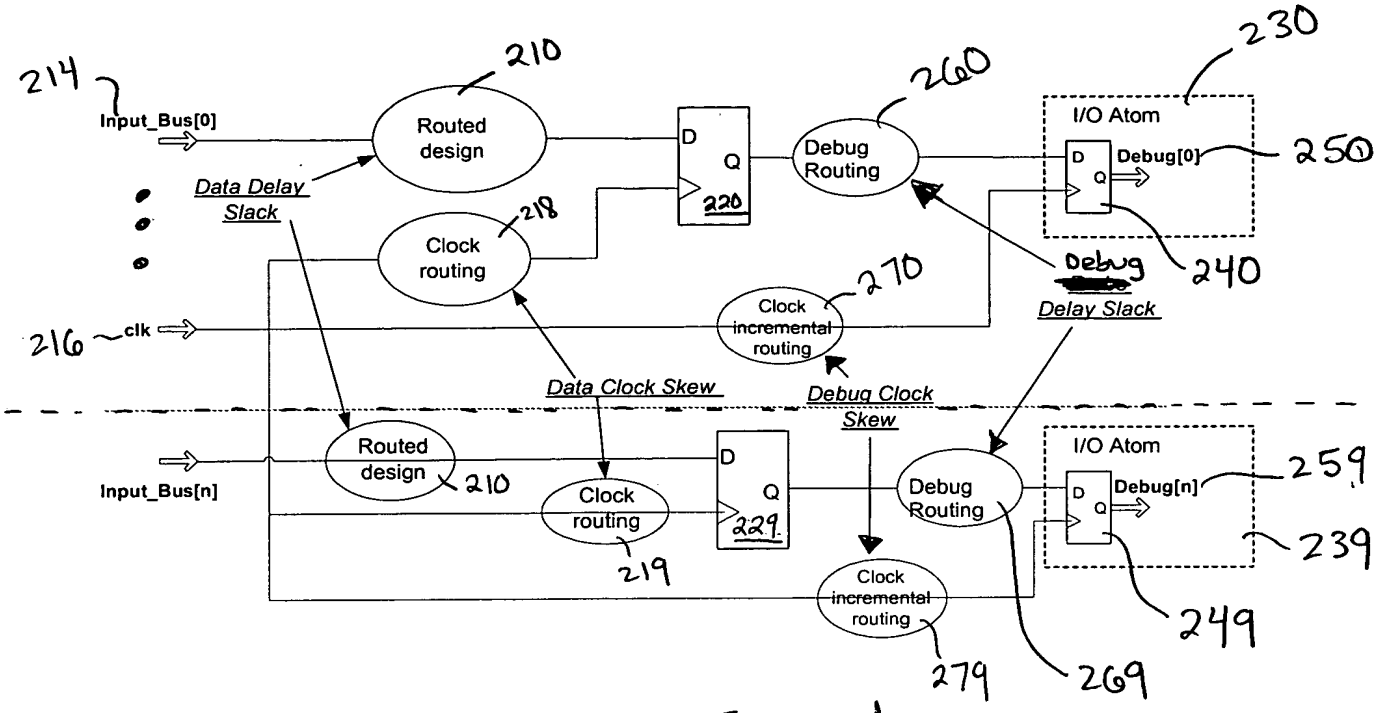
FIG. 1 (prior art)





100

FIG. 2

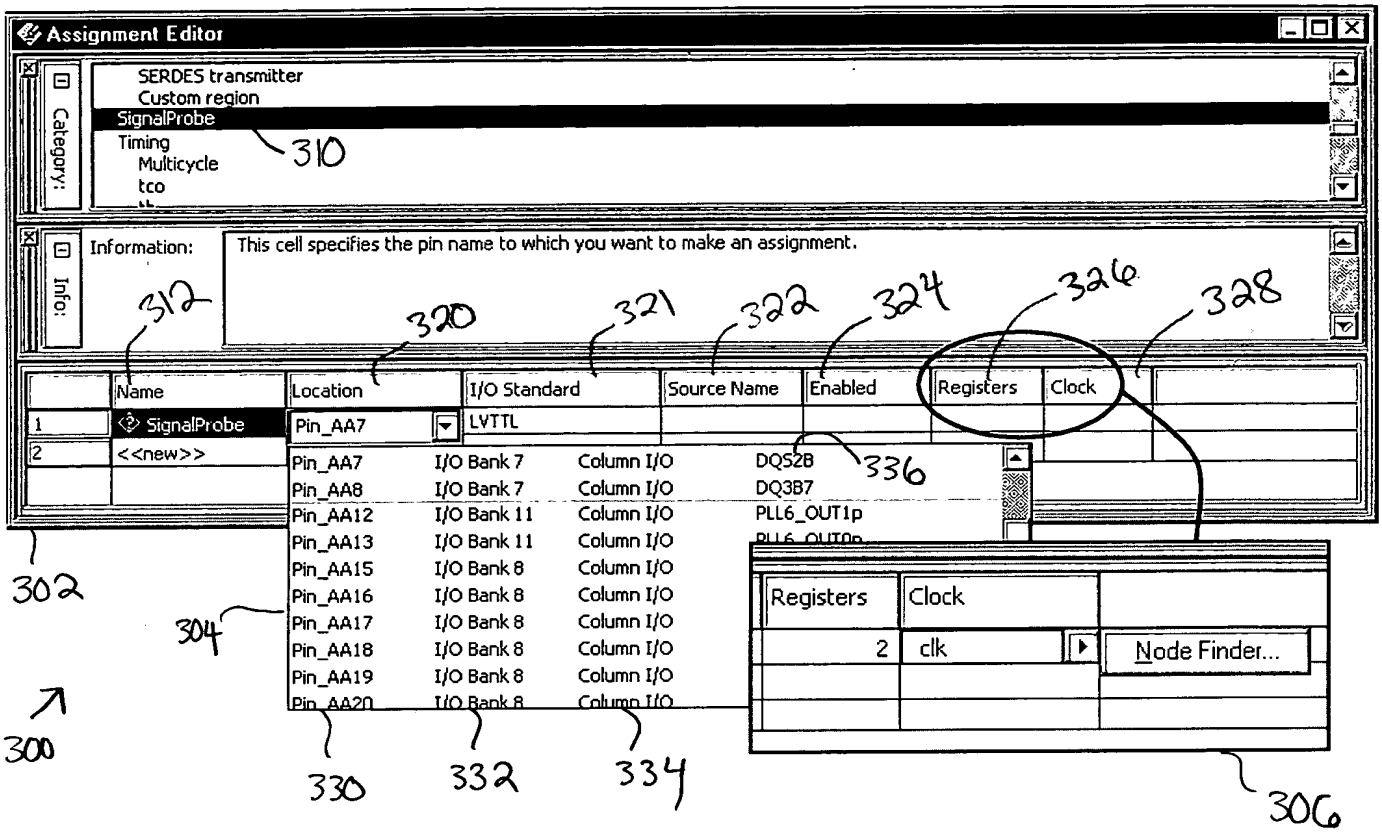


Debugging Example

200

FIG. 3

FIG. 4 User Interface Example



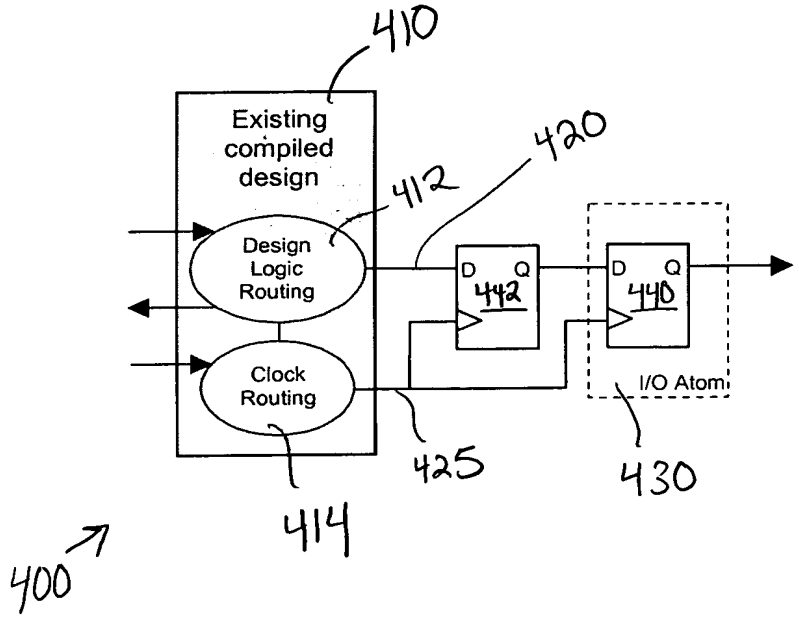
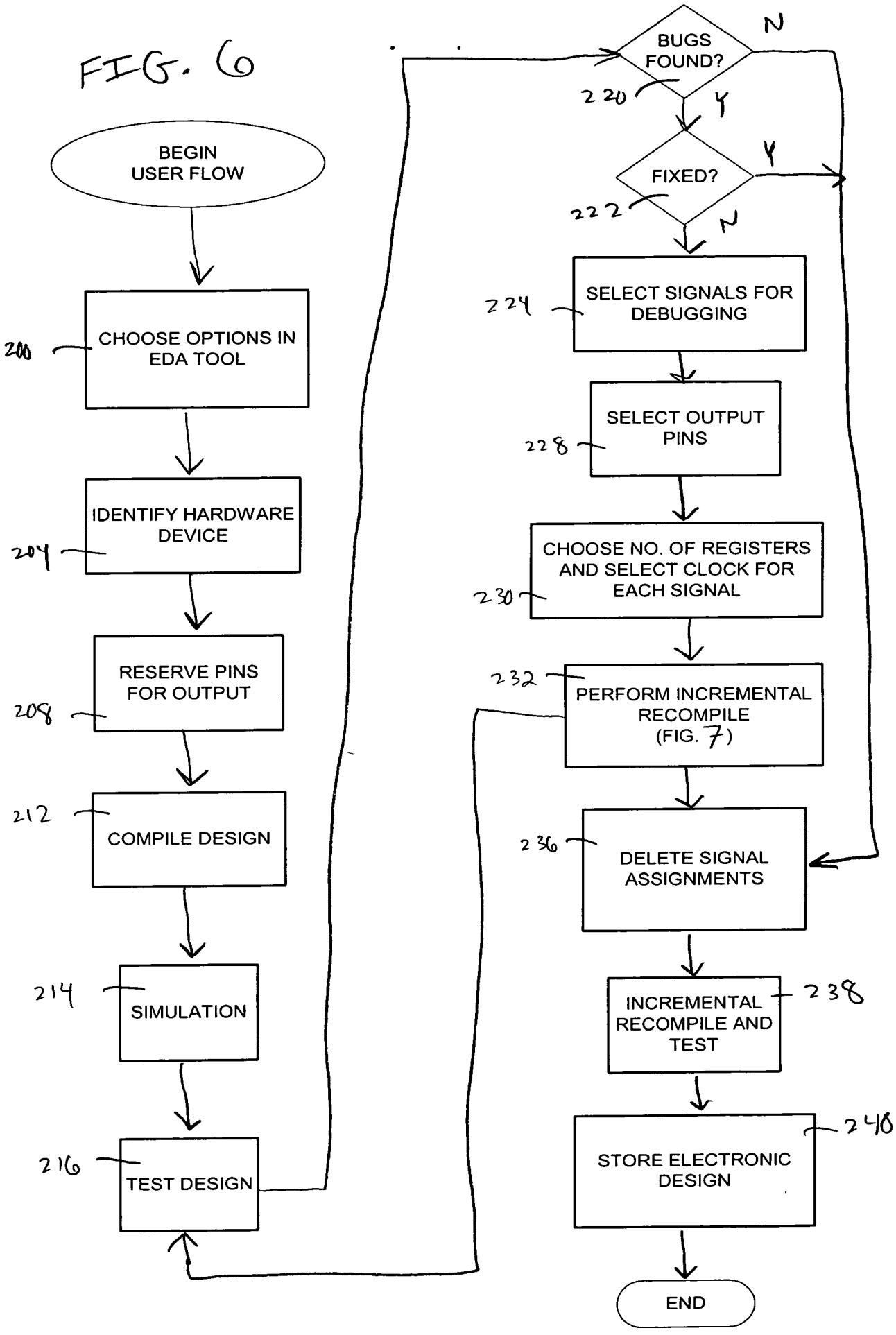


FIG. 5

Debugging Example

FIG. 6


BEGIN USER FLOW
200
CHOOSE OPTIONS IN EDA TOOL
204
IDENTIFY HARDWARE DEVICE
208
RESERVE PINS FOR OUTPUT
212
COMPILE DESIGN
214
SIMULATION
216
TEST DESIGN
220
BUGS FOUND?
N
Y
222
FIXED?
Y
N
224
SELECT SIGNALS FOR DEBUGGING
228
SELECT OUTPUT PINS
230
CHOOSE NO. OF REGISTERS AND SELECT CLOCK FOR EACH SIGNAL
232
PERFORM INCREMENTAL RECOMPILE (FIG. 7)
236
DELETE SIGNAL ASSIGNMENTS
238
INCREMENTAL RECOMPILE AND TEST
240
STORE ELECTRONIC DESIGN
END

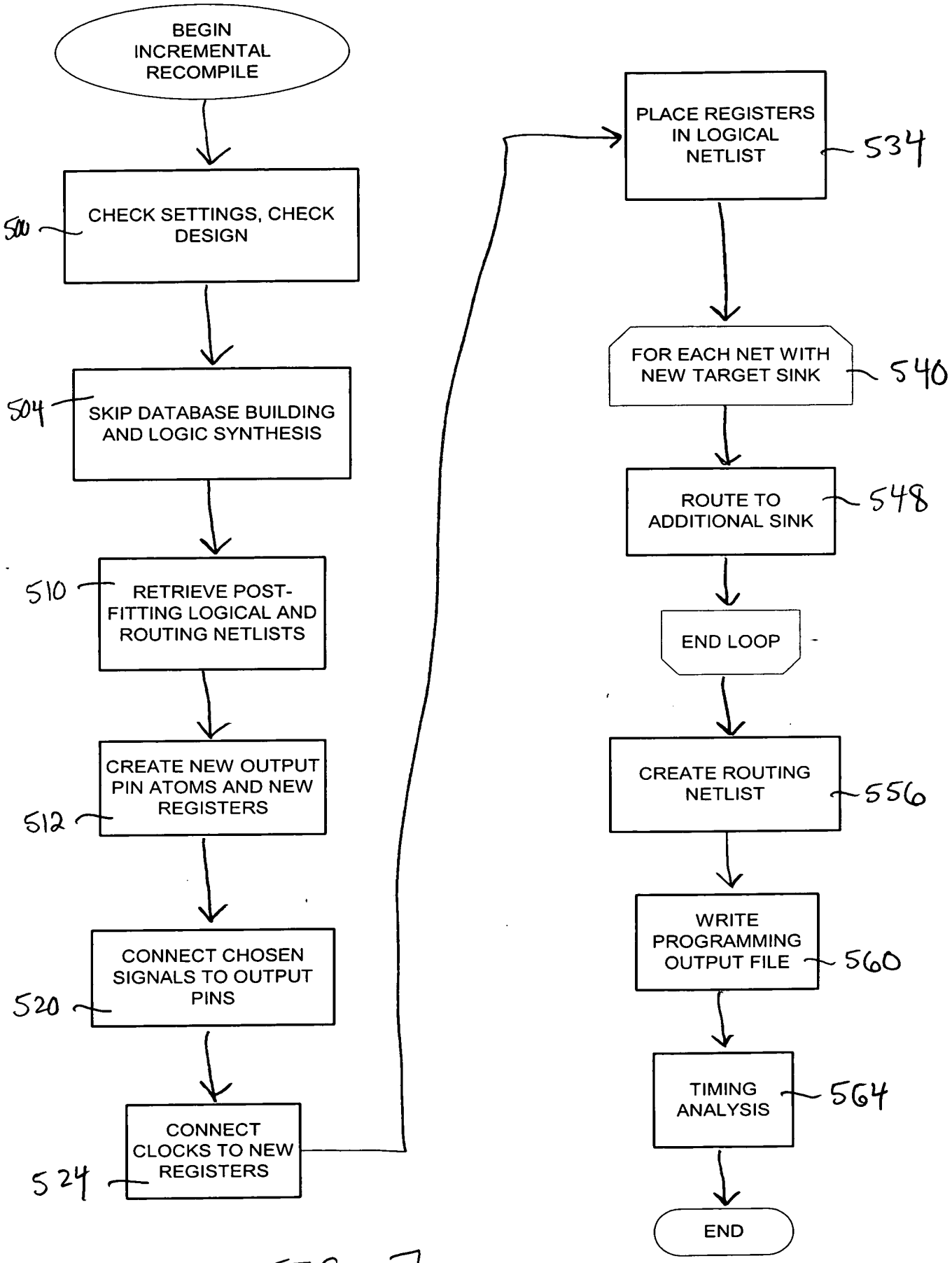

BEGIN INCREMENTAL RECOMPILE
CHECK SETTINGS, CHECK DESIGN
500
SKIP DATABASE BUILDING AND LOGIC SYNTHESIS
504
RETRIEVE POST-FITTING LOGICAL AND ROUTING NETLISTS
510
CREATE NEW OUTPUT PIN ATOMS AND NEW REGISTERS
512
CONNECT CHOSEN SIGNALS TO OUTPUT PINS
520
CONNECT CLOCKS TO NEW REGISTERS
524
PLACE REGISTERS IN LOGICAL NETLIST
534
FOR EACH NET WITH NEW TARGET SINK
540
ROUTE TO ADDITIONAL SINK
548
END LOOP
CREATE ROUTING NETLIST
556
WRITE PROGRAMMING OUTPUT FILE
560
TIMING ANALYSIS
564
END

FIG. 7

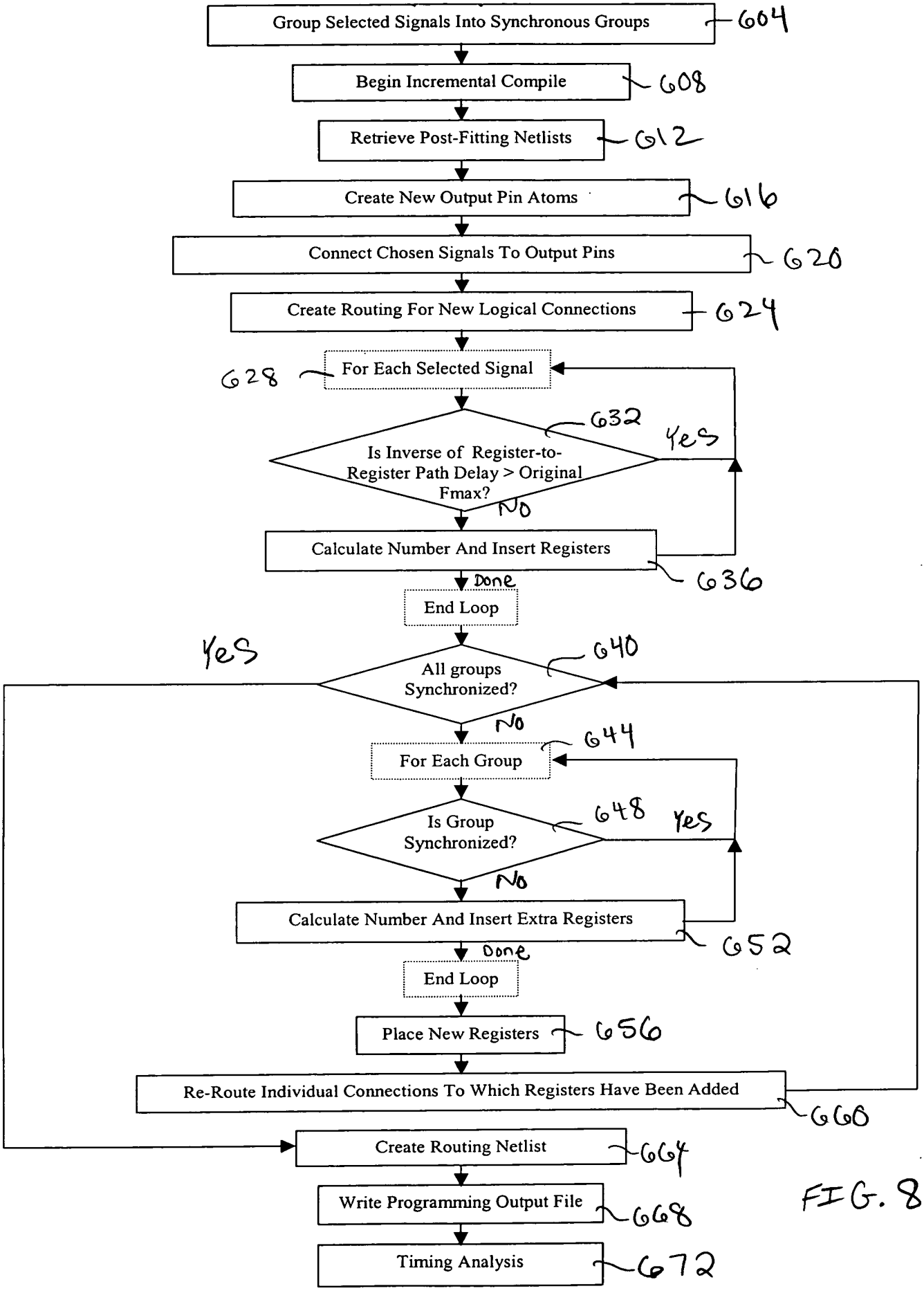
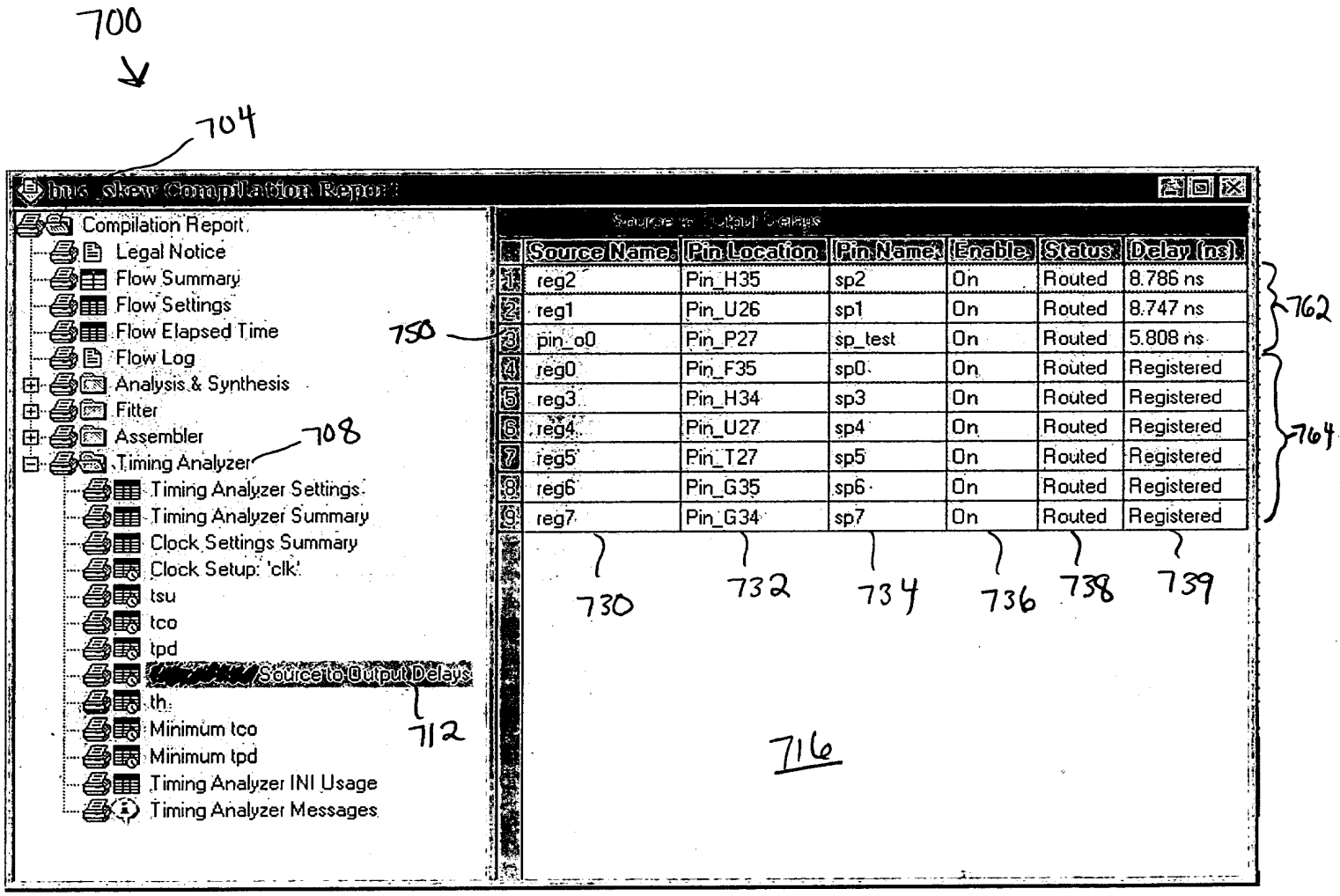

Group Selected Signals Into Synchronous Groups
604
Begin Incremental Compile
608
Retrieve Post-Fitting Netlists
612
Create New Output Pin Atoms
616
Connect Chosen Signals To Output Pins
620
Create Routing For New Logical Connections
624
For Each Selected Signal
628
Is Inverse of Register-to-Register Path Delay > Original Fmax?
632
Yes
No
Calculate Number And Insert Registers
636
Done
End Loop
All groups Synchronized?
640
Yes
No
For Each Group
644
Is Group Synchronized?
648
Yes
No
Calculate Number And Insert Extra Registers
652
Done
End Loop
Place New Registers
656
Re-Route Individual Connections To Which Registers Have Been Added
660
Create Routing Netlist
664
Write Programming Output File
668
Timing Analysis
672

FIG. 8

FIG. 9

Timing Report Table



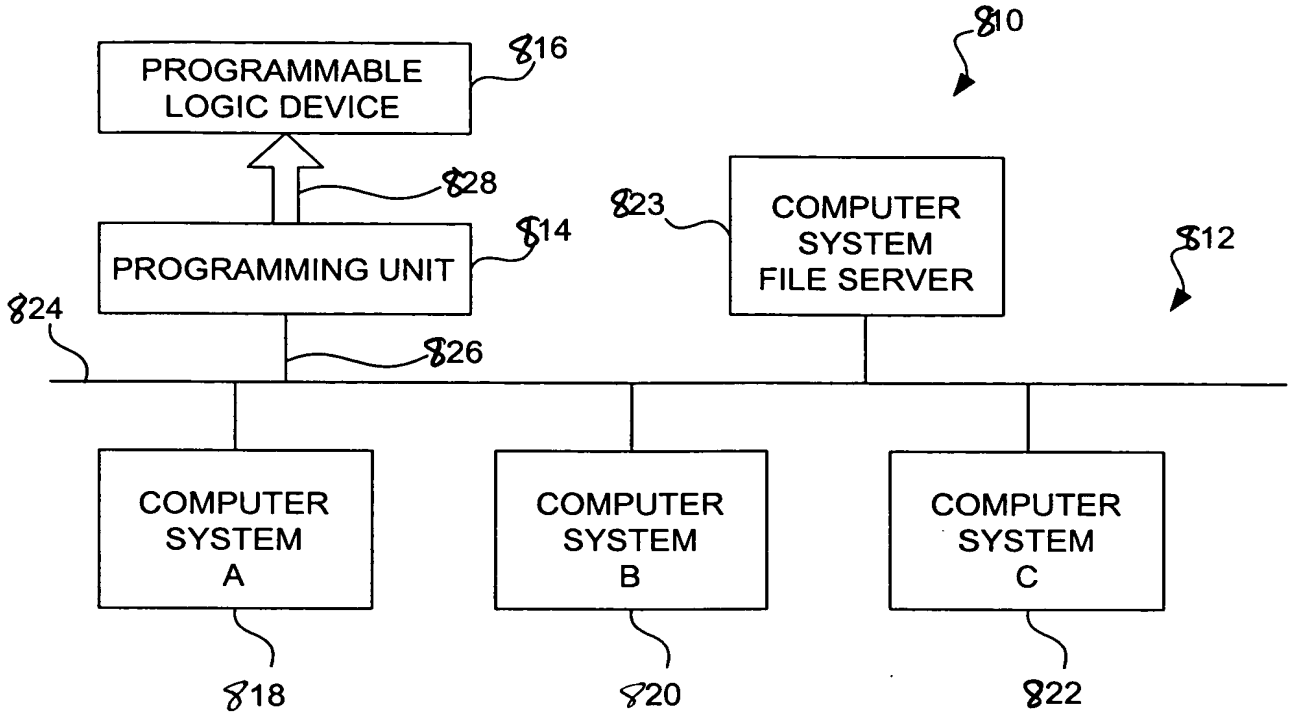

PROGRAMMABLE LOGIC DEVICE
816
810
828
823
COMPUTER SYSTEM FILE SERVER
814
812
PROGRAMMING UNIT
824
826
COMPUTER SYSTEM A
COMPUTER SYSTEM B
COMPUTER SYSTEM C
818
820
822

FIG. 8 10

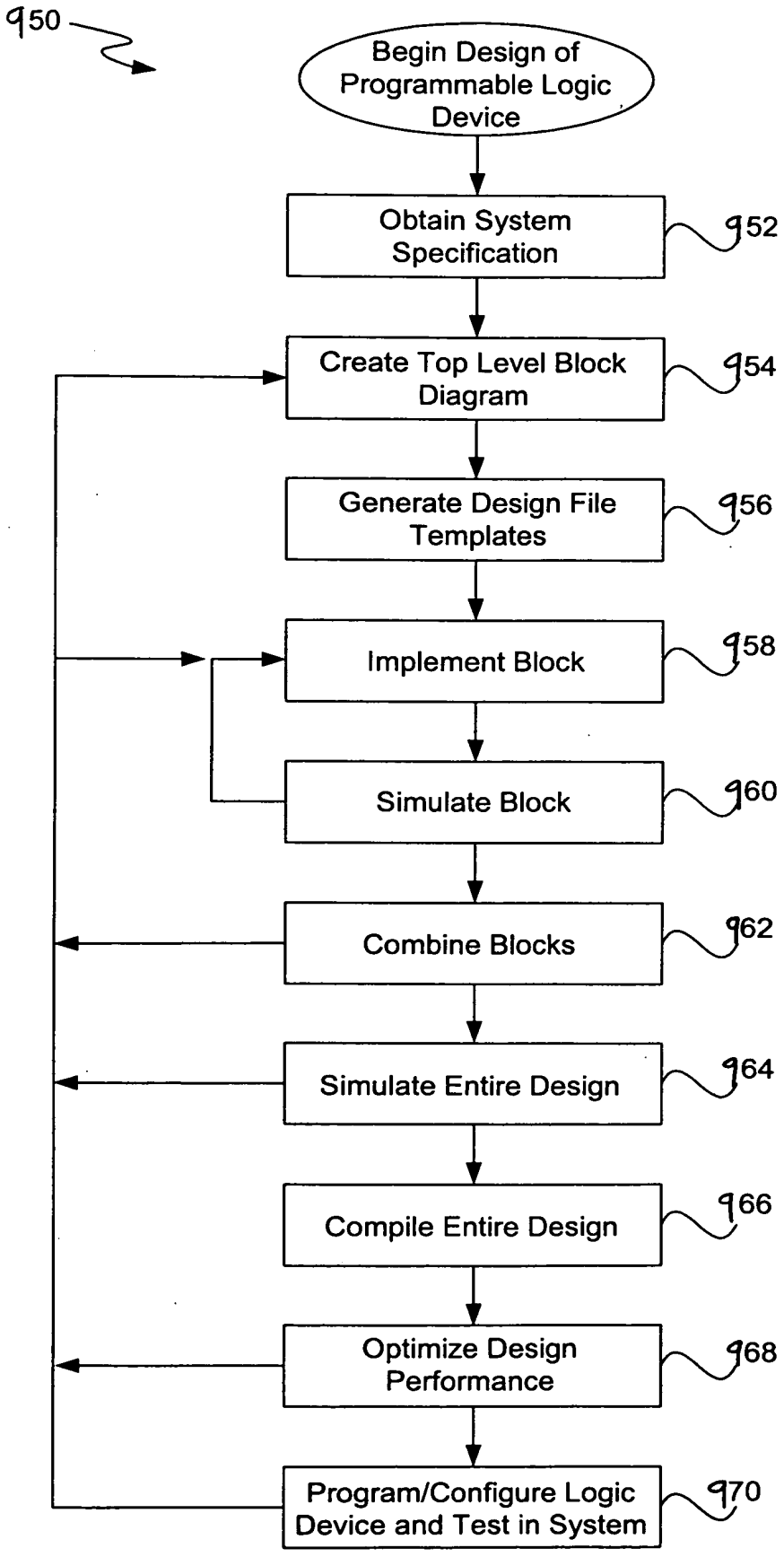

950
Begin Design of Programmable Logic Device
Obtain System Specification
952
Create Top Level Block Diagram
954
Generate Design File Templates
956
Implement Block
958
Simulate Block
960
Combine Blocks
962
Simulate Entire Design
964
Compile Entire Design
966
Optimize Design Performance
968
Program/Configure Logic Device and Test in System
970

FIG. 11

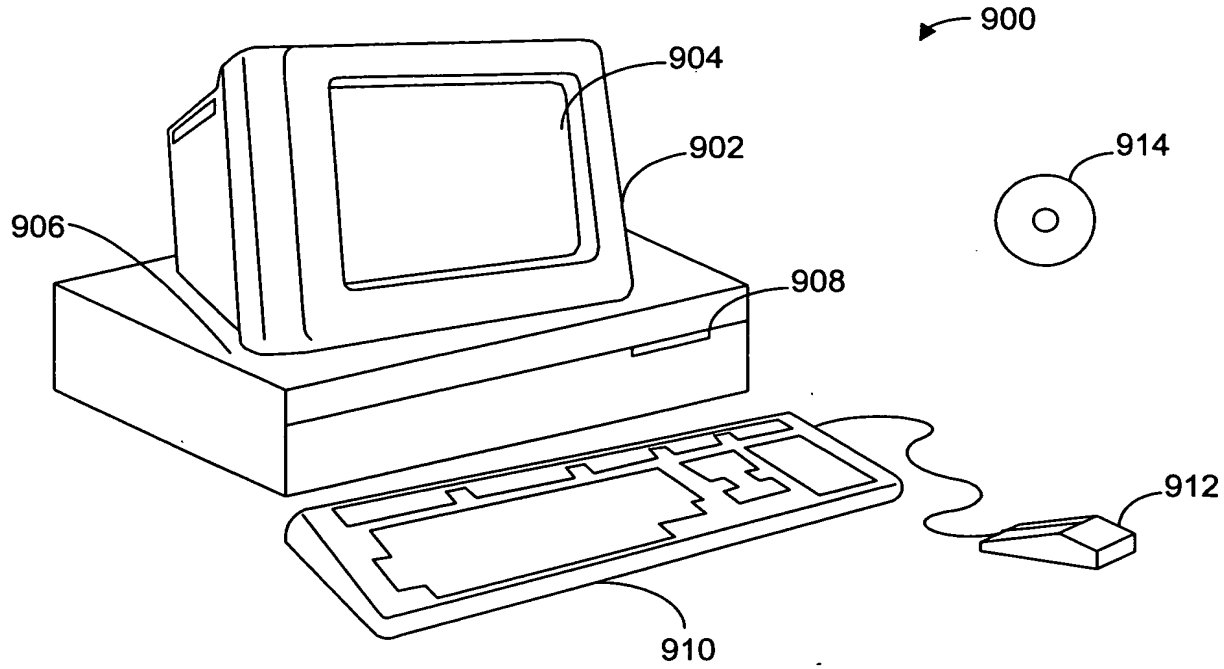


FIG. 12A

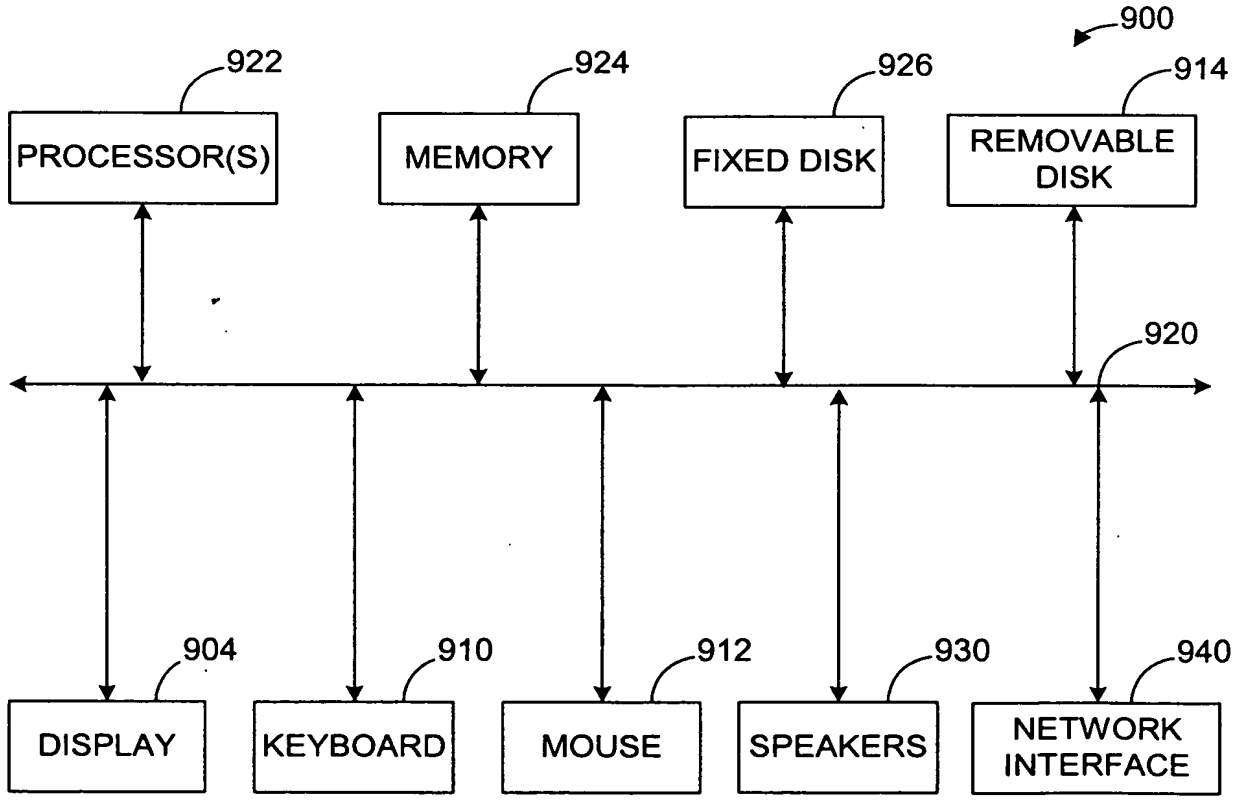


FIG. 12B